Figs. 17AA to 17AD and Figs. 17BA to 17BD are cross sectional views of a semiconductor substrate illustrating analysis on how etching occurs.

Figs. 18AA to 18AD and Figs. 18BA to 18BD are cross sectional views of a semiconductor substrate illustrating analysis on how etching occurs.

IN THE CLAIMS:

CANCEL claim 2 and 8-18 without prejudice or disclaimer.

AMEND claims 1 and 4 as follows:

1. (Amended) A semiconductor device comprising:

an underlie having a conductive region in a surface layer of said underlie;

an insulating etch stopper film covering a surface of said underlie;

an interlayer insulating film formed on said insulating etch stopper film;

a wiring trench formed in said interlayer insulating film, said wiring trench having a bottom surface at a first depth from a surface of said interlayer insulating film, and a side wall;

a contact hole extending from said bottom surface of said wiring trench to a surface of the conductive region through a remaining thickness of said interlayer insulating film and through said insulating etch stopper film; and

a dual damascene wiring layer embedded in said wiring trench and in said contact hole,

wherein said interlayer insulating film includes a first kind of an insulating layer surrounding a side wall and the bottom surface of said wiring trench and a second kind of an insulating layer disposed under the first kind of the insulating layer and having etching characteristics different from the first kind of the insulating layer, and

wherein said contact hole has an upper portion whose cross sectional area gradually increases toward an upper level and reaches the bottom surface of said wiring trench in the first kind of the insulating layer.

4. (Amended) A semiconductor device according to claim 3, wherein said contact hole has a portion whose cross sectional area gradually increases from an intermediate level of the second kind of the insulating layer toward an upper level and reaches the bottom surface of said wiring trench.

ADD the following new claims 19-26:

19. (New) A semiconductor device according to claim 1, wherein said interlayer insulating layer has a shoulder at said portion, which extends from said bottom surface into said second kind of the insulating layer.

20. (New) A semiconductor device according to claim 19, wherein said shoulder is smoothly continuous with the bottom surface.

21. (New) A semiconductor device according to claim 20, wherein said shoulder is formed by etching from above and from said contact hole.

22. (New) A semiconductor device according to claim 1, wherein said interlayer insulating has a rounded shoulder at said portion.

23. (New) A semiconductor device according to claim 22, wherein said shoulder extends from said bottom surface in the first kind of the insulating layer to an intermediate position of the contact hole in said second kind of the insulating layer.

24. (New) A semiconductor device according to claim 1, wherein said contact hole has a generally vertical side wall in a lower part, and a gently sloped shoulder in an upper part.

25. (New) A semiconductor device according to claim 1, wherein said first kind of the insulating layer is made of fluorine-containing silicon oxide, and said second kind of the insulating layer is made of silicon oxide.

AP Cont.

26. (New) A semiconductor device according to claim 3, wherein said first kind of the insulating layer is made of fluorine-containing silicon oxide, said second kind of the insulating layer is made of silicon nitride, and the third kind of the insulating layer is made of fluorine-containing silicon oxide.